Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **1A**
2. **1B**
3. **1Y**
4. **2A**
5. **2B**
6. **2Y**
7. **GND**
8. **3Y**
9. **3A**
10. **3B**
11. **4Y**
12. **4A**
13. **4B**
14. **VCC**

**042”**

**.055”**

**MASK**

**REF**

**F38**

**1 14 13**

**2 12**

**3 11**

**4 10**

**5 9**

**6 8**

**7**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential:**

**Mask Ref: F38**

**APPROVED BY: DK DIE SIZE .042” X .055” DATE: 6/28/22**

**MFG: TEXAS INSTRUMENTS THICKNESS .025” P/N: 54F38**

**DG 10.1.2**

#### Rev B, 7/1